

App. Serial No. 10/511,512
Docket No.: NL020321US

In the Abstract:

Please amend the abstract as indicated below.

A multi-issue processor ~~comprises~~ includes a register file and a plurality of issue slots (~~UC₀, UC₁, UC₂ and UC₃~~), each one of the plurality of issue slots having a plurality of functional units (~~FU₀, FU₁ and FU₂~~) and a plurality of holdable registers (~~1-33 and 101-117~~). The plurality of issue slots ~~comprises~~ include a first set of issue slots (~~UC₁, UC₂ and UC₃~~) and a second set of issue slots (~~UC₀~~), and the register file (~~RF₀ and RF₁~~) is accessible by the plurality of issue slots (~~UC₀, UC₁, UC₂ and UC₃~~). A location of at least a part of the plurality of holdable registers (~~1-33~~) in the first set of issue slots (~~UC₁, UC₂ and UC₃~~) is different from a location of at least a corresponding part of the plurality of holdable registers (~~101-117~~) in the second set of issue slots (~~UC₀~~). ~~The holdable registers can prevent that the inputs of unused functional units change, which would result in unnecessary power dissipation. However, this increases the amount of state that has to be saved during interrupt handling. By varying the position of the holdable registers for different issue slots, less state saving may be required during interrupt handling, while maintaining a significant reduction in power consumption and improved performance.~~